Efficient process development for bulk silicon etching using cellular automata simulation techniques

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ABSTRACT

This paper describes cellular automata simulation techniques used to predict the anisotropic etching of single-crystal silicon. In particular, this paper will focus on the application of wet etching of silicon wafers using typical anisotropic etchants such as KOH, TMAH, and EDP. Achieving a desired final 3D geometry of etch silicon wafers often is difficult without requiring a number of fabrication design iterations. The result is wasted time and resources. AnisE, a tool to simulate anisotropic etching of silicon wafers using cellular automata simulation, was developed in order to efficiently prototype and manufacture MEMS devices. AnisE has been shown to effectively decrease device development time and costs by up to 50% and 60%, respectively.

Keywords: Anisotropic etch simulator, bulk micromachining, silicon, CAD, MEMS

1. INTRODUCTION

The recent growth in the number of MEMS devices that are being fabricated using bulk silicon etching technology has necessitated efficient design and development. It is often difficult to predict the result of etching single-crystal silicon with typical wet etchants such as KOH, TMAH, and EDP due to the anisotropic nature of the etching that is taking place. Etching rates for a given temperature and concentration of the etchant are not the same for the different silicon crystal planes. Figure 1 shows a graphical representation of the silicon etch rate dependence on the crystalline plane, etchant temperature, and etchant concentration. As the complexity of mask increases and the time of the etching increases, it becomes increasingly difficult to predict the final 3D geometry based on heuristics.

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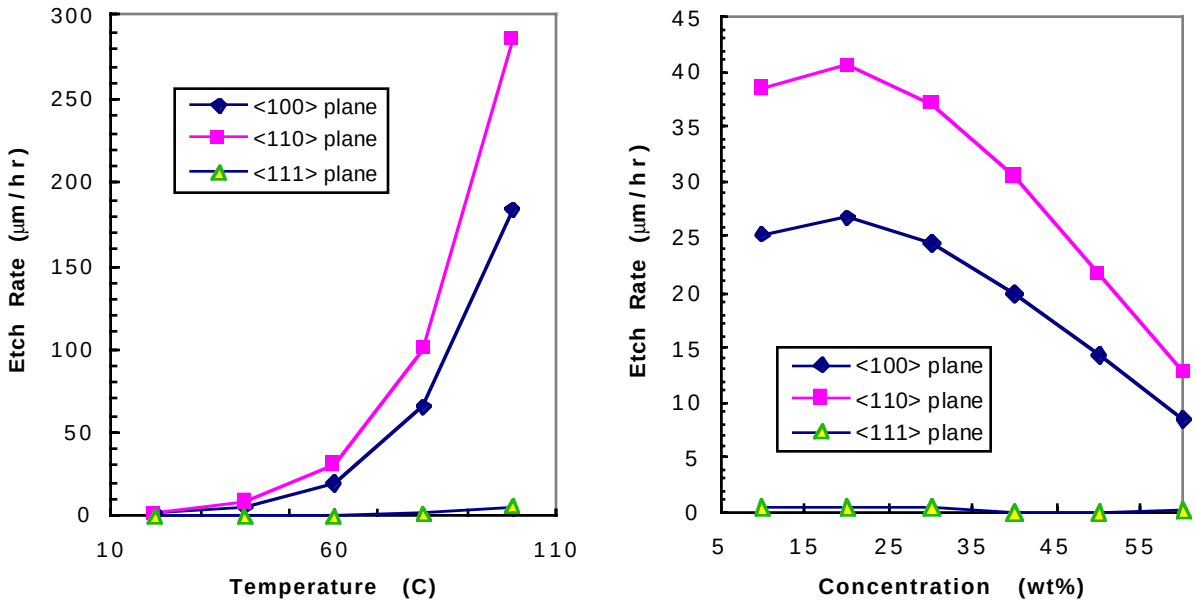


Figure 1: Silicon etch rate as a function of temperature at fixed concentration of 40% (left), silicon etch rate as a function of concentration at fixed temperature of 60°C (right). [1]

The use of a bulk silicon etch simulator to predict the 3D geometry of etched structures has successfully aided in producing optimized masks designs. These optimized designs have reduced the number of microfabrication test iterations that are required before desired etch features are realized.

2. AnisE DEVELOPMENT

IntelliSense has developed an anisotropic etch simulator to reduce the burden of microfabrication. It was developed so that users could customize and tailor the results to their specific process. This simulator was made commercially available to the MEMS community last year and is known as AnisE™.

The AnisE code was developed using the Cellular Automata model. This general model is based on a discretized domain of cells or repeated components. This model can closely represent the actual atomic-level etching of silicon. Figure 2 shows the crystal structure of silicon. The development of the etch simulator is based on this crystalline geometry,

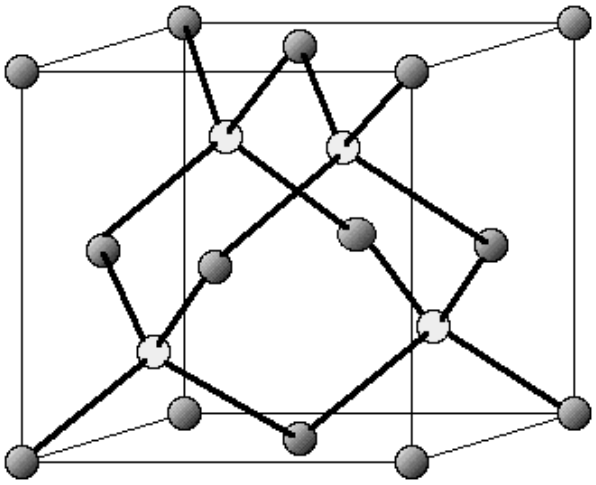


Figure 2: Silicon crystal structure.

Within the cellular domain, a number of rules and conditions are established.

The cellular automata model is dependent on:

- The lattice structure of the cells,
- The possible states of a cell,
- The effect of neighboring cell, and
- The rules to determine the state of the cell.

Lattice structure
For bulk silicon etch simulation, the silicon crystal structure is chosen as the lattice of the cellular automaton. AnisE does not simulate the etching of silicon at an atomic-scale since the simulation would be computationally too intense even for supercomputers. Instead, a silicon atom is represented by a cell in the model in terms of its lattice configuration. The size of each cell is on the order of $1\mu m^3$ depending on the selected resolution of the model.

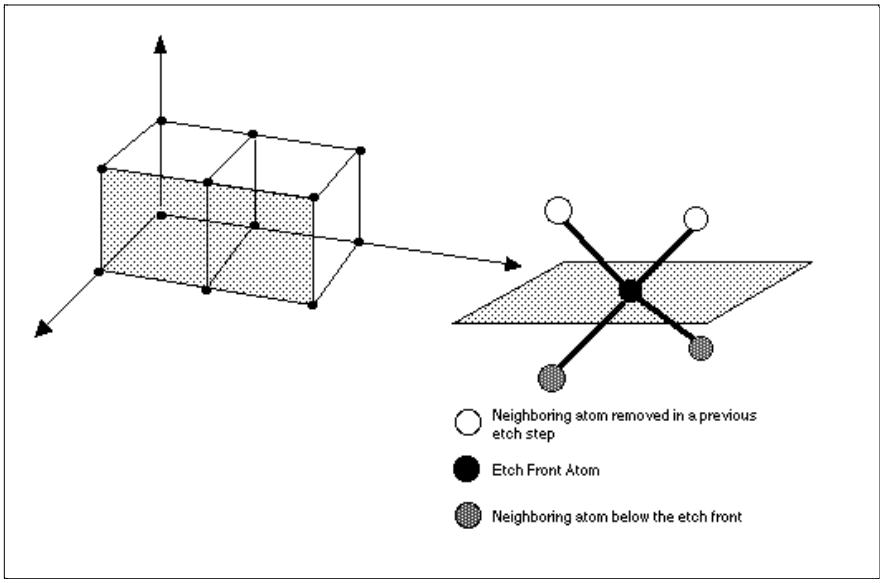
States of cell
Each cell corresponds to a silicon atom in the silicon crystal structure. Cellular Automata predicts the etch profile by determining the probability that certain cells will be "etched" or "not etched." These are the two possible states of the cells.

Effect of neighboring cells
Each of the cells state depends on its local interaction with four other cells. This configuration was chosen to mimic the silicon crystal in which each silicon atom is covalently bonded to four other neighboring atoms. Similarly, the behavior of each atom depends on its local interaction with its neighboring atoms.

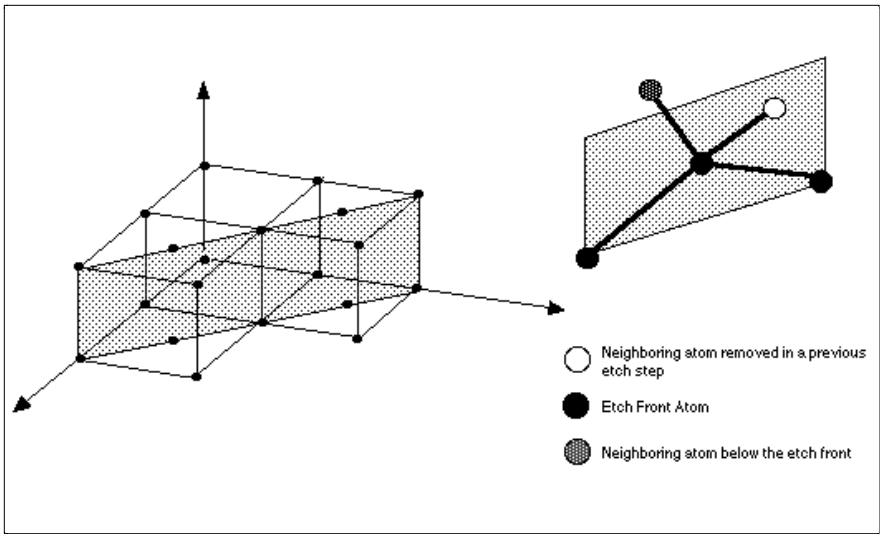
Rules to determine the state of the cell.
The rules to determine the state of the cell depend on the conditions of the other cells that are surrounding it. Considering crystal silicon for example, the location and number of covalent silicon bonds that must be broken in order to remove an atom from the lattice has a large impact on that atom's susceptibility of being removed, or etched. For determining these

rules, the <100>, <110> and <111> silicon crystal planes will be considered. In principle, higher order planes such as <311>, <411>, etc., can be incorporated into the model, as well.

Figure 3 shows a representation of the three silicon planes mentioned above. The plane shown on the right in the figures represents the etch front of the crystal lattice.



(a)



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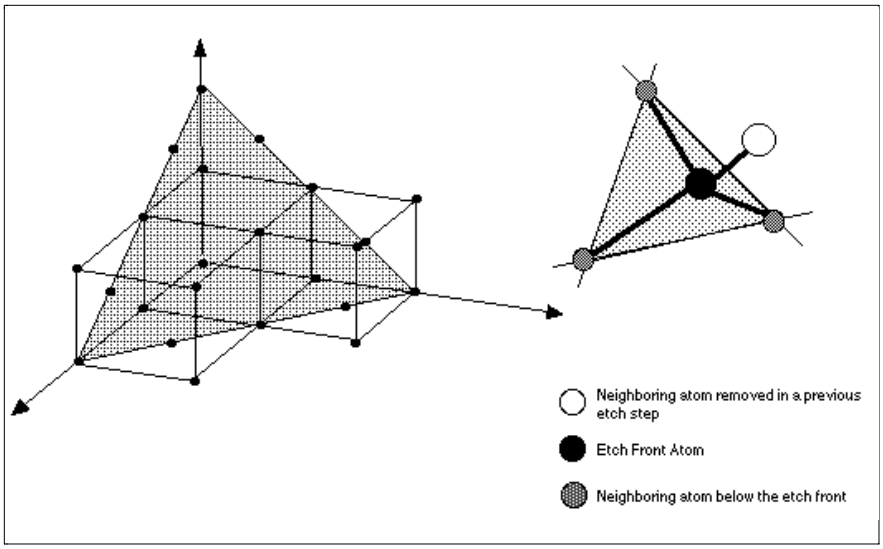

(c)

Figure 3: the cells/atoms contained in the <100>, <110>, and <111> silicon crystal planes, (a), (b), and (c), respectively. [2]

When considering the etch front cell for the <100> plane as shown in Figure 3a, it can been seen that in order to expose this cell, two neighboring cells must be removed. That is, in the previous etch step, two neighboring cells were removed. In addition, it can be seen that in order to remove the cell from the crystal lattice, two covalent bonds must be broken. These bonds lie below the etch-front plane.

When considering the etch front for the <110> plane in Figure 3b, there are three etch-front atoms. In order to expose these cells, only one neighboring cells must be removed in the previous step. In order to remove any of these cells from the crystal lattice, three covalent bonds must be broken. It is important to note that two of these three bonds lie in the etch front plane, thus making them easier to break.

Finally, for the <111> plane, there is only one etch-front atom. One neighboring cell must be etched in a previous step to expose the etch-front atom. In order to remove this cell, three covalent bonds must be broken. Each of these three covalent bonds lie below the etch-front plane.

From the above orientations of the cells with respect to the planar etch front, the probability is calculated whether the cell will be removed. This probability takes into account the experimental silicon etch rates for the <100>, <110>, and <111> etch planes. A higher etch rate for a given etch plane will increase the probability that the etch-front atom in that plane will be removed.

It is important to note that this model implicitly considers the second order effects resulting from the second nearest neighbors. This is the case since the model takes into account the number of neighboring cells and also their location with respect to the etch front. As a result, the simulation predicts the appearance of higher order etch planes.

3. AnisE OPERATION

AnisE was developed to require the least amount of user input while insuring accurate simulation results. The AnisE interface is intuitive, and users must define the following minimum set of information:

- Etchant type (KOH, TMAH, EDP),
- Etchant temperature and concentration,
- Mask layout (via internal mask editor, DXF, or GDS II formats),
- Wafer orientation (<100> or <110>), and
- Etch time

Once the etchant type, temperature, and concentration are specified, an etch rate database is accessed which provides the silicon etch rates for the primary Miller Indices, <100>, <110>, and <111>. In addition, users have the option of inputting their own etch rate information if they prefer not to use the database defaults. These etch rates along with the mask which defines protected areas on the silicon, are used as inputs into the cellular automata model. Figure 4 shows the AnisE user interface.

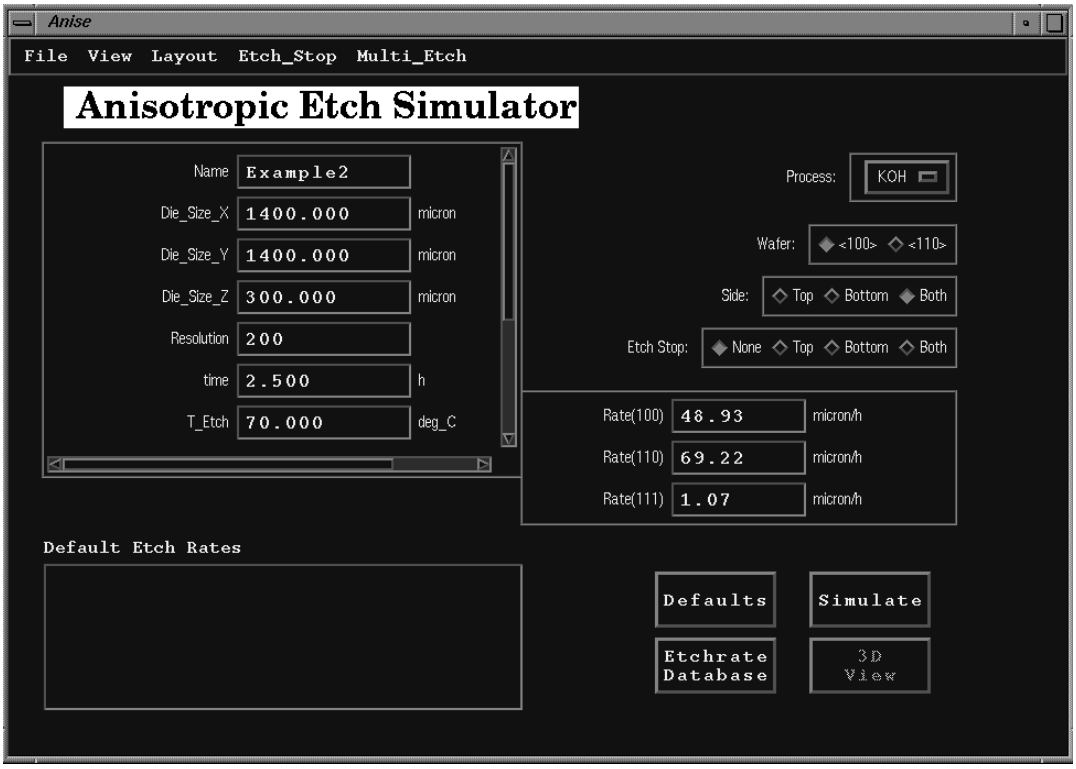

Figure 4: AnisE user-interface.

In order to successfully cover a wider range of problems, AnisE was developed with additional capabilities to handle double sided etching, etch stops, and multi-process etching. The technical details of these features are not discussed in this paper.[3]

4. EFFICIENT DEVICE DESIGN

AnisE is used in-house by IntelliSense and by organizations around the world developing products via anisotropic etching of silicon. Comparisons of simulated results to SEMs of etched structures show very good accuracy. Etch depths and feature sizes are captured accurately by the simulation. The number of microfabrication test iterations needed for bulk silicon etching has been reduced in facilities that utilize this etch simulation method.

Example 1: Undercutting prediction

The purpose of this simulation and experiment was to determine the extent of undercutting for a given set of etch parameters. Figure 5a shows the mask layout that was created with AutoCAD in the DXF file format. The mask x and y dimensions are approximately 2500µm by 2600µm.The actual and simulated conditions for this example were as follows: temperature 50ºC, etch time 14 hours and 20 minutes, concentration 31% KOH, and <100> orientation.

The DXF mask file was imported directly into AnisE for etch simulation. Figure 5b shows the AnisE simulation results, and Figure 6 shows a SEM photo of the etched structure. After one fabrication iteration was performed, a comparison of results showed that AnisE correctly predicted the undercutting.[4]

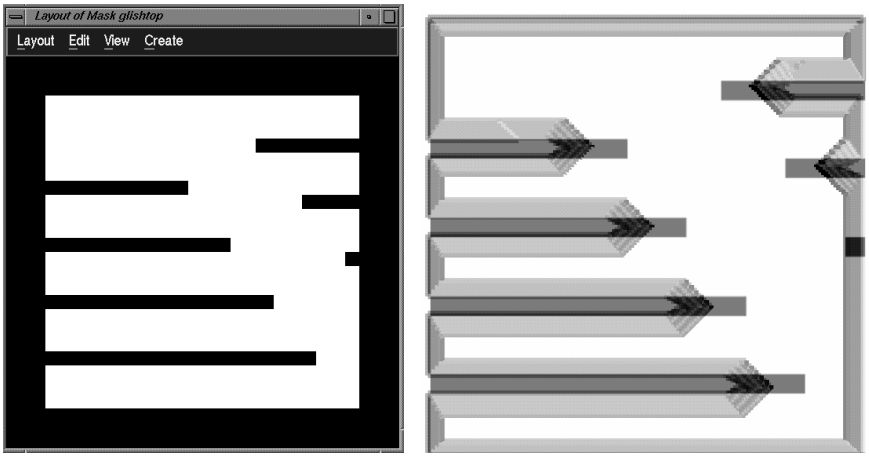

Figure 5: (a) Mask layout and (b) predicted AnisE results (shown with overlaid mask).

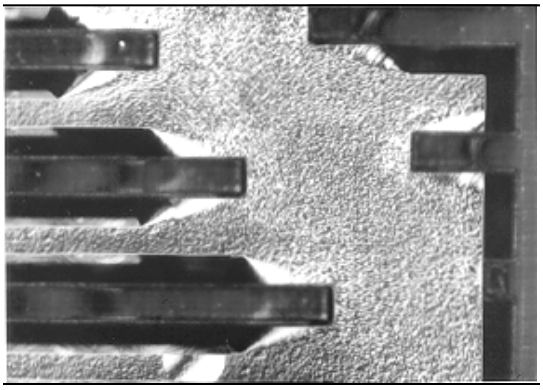

Figure 6: SEM of etched structure (close-up).

Example 2: Corner compensation

An optical device currently being manufactured was designed using the AnisE software. The device was built via bulk etching of a <100> silicon wafer with KOH. It was desired that the feature being etched have a square corner in order to maximize the top surface area. Figures 7 and 8 show comparisons of AnisE simulations to SEMs at different etch times.

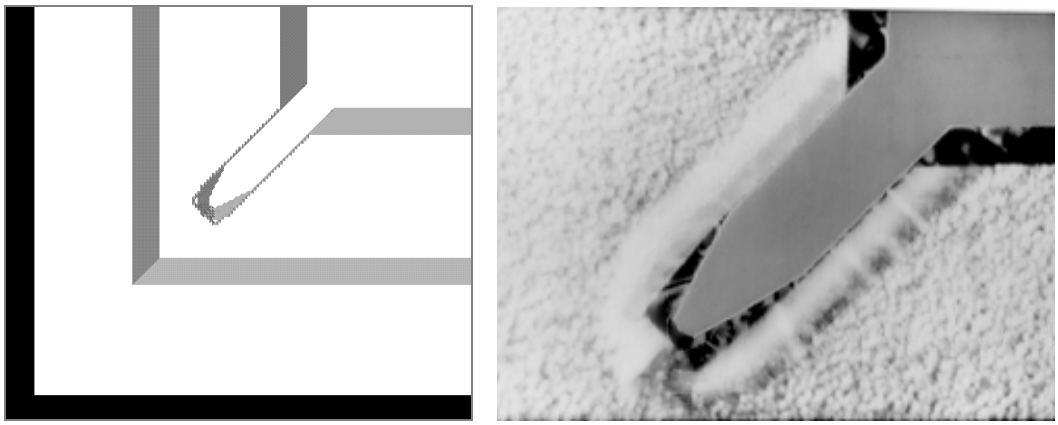

Figure 7: AnisE simulation (left) and etch results (right) at 40% completion.

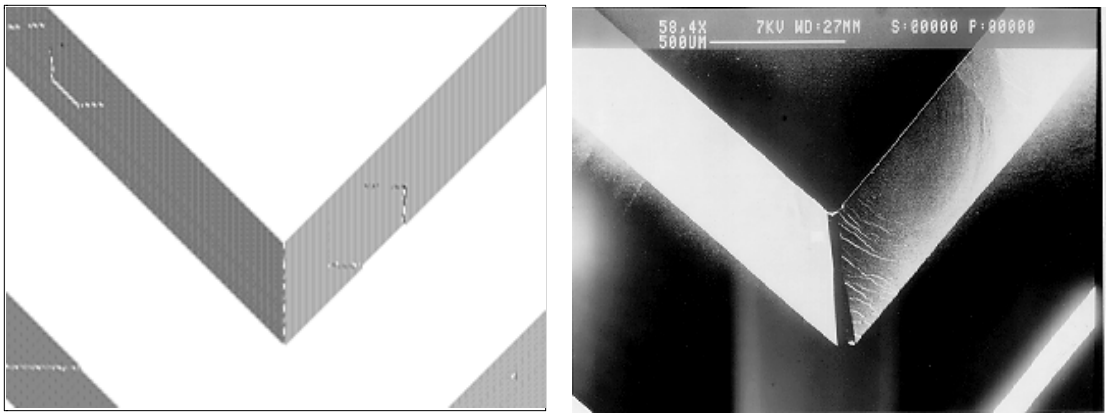

Figure 8: AnisE simulation (left) and etch results (right) at 100% completion.

For this example, AnisE was used to successfully predict the etching results (in terms of etch depth and corner rounding) to within 4 %. Other similar corner compensation examples show accuracy to within 7%.[4]

Time and cost reduction:

Typically, process development for standard bulk etching requires months of development time and require substantial expenditure. In the process development, an average of 3-4 test iterations are usually required before a desired design is obtained. [4]

Alternatively, when AnisE has been used to first optimize the mask design, the desired design can be obtained quicker - often in one test iteration. A design and process development cycle is typically 50% shorter and 60% less expensive when AnisE is used.[4]

5. CONCLUSIONS

As more silicon bulk-etched devices are being manufactured and sold, improvements in design optimization and process development efficiency will be desired. AnisE is a silicon etch simulator developed to address this need for efficient device design. By modeling the silicon wafer as a discrete set of cells that represent the silicon crystalline structure, accurate predictions of 3D results can be made quickly on a computer.

By simulating etching prior to prototyping, AnisE has been shown to effectively decrease development time and costs by up to 50% and 60%, respectively.

6. ACKNOWLEDGMENTS

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7. REFERENCES

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