MEMS
Extraction & verification
What is extraction?

Simplifying a full 3D model into behavioral model

- Convert FEA/BEA model (large DOFs) into computationally efficient model
- Develop pre-computed energy based model that captures multiphysics

What is extracted?

- Mechanical Strain Energy of Modes of Interest (including stress and stress gradient effects)
- Capacitive energy
- Thermal effects (deformation due to temperature change)
- Fluidic Structure Interaction (due to compressive or non-compressive media)
- Other dissipation sources (thermoelastic damping (v8.6.1) and anchor acoustic losses (v8.6.2))
System Model Extraction (SME)

1. Capture total energy of relevant mode (Mechanical, Electrostatic, Dissipation)
2. Krylov/Arnoldi methods to generate Lagrangian formulation
3. Create Compact model for system modeling
System model extraction (SME) flow chart

Summary: Convert problem from Newtonian (inertia based) to more efficient Lagrangian domain (energy based)
SME advantages

- Automated full multi-physics capture
- 1000 X faster than pure FEA
- Matches FEA to within 1% accuracy
- Fully capture harmonic responses
- 3D MEMS system simulation
- Device and package level extraction
- Automated VHDL/Verilog/SPICE generation
EDA Linker capabilities (compatibility)

- Create accurate N-DOF dynamic system model from MEMS FEA/BEA model
- Output system model into SPICE, HDL, and Simulink formats
- Compatible with EDA tools from Cadence, Mathworks, Mentor, Synopsys and Tanner
- Integrated CMOS-MEMS (SoC/SiP) compatibility
Integrated design flow for MEMS + IC

1. Device/System Design Exploration
   Design of Experiments (SYNPLE/IntelliSuite)

2. Final MEMS Device design
   (Multiphysics)

3. N-DOF Lagrangian System Model Extraction
   (IntelliSuite)

4. Transistor level design
   (SPICE/SYNPLE or other EDA tools)

5. Gate level
   Place and route, DRC, LVS
   (Cadence/Synopsys/Mentor/ViewLogic/Tanner etc)

6. Final Layout
   (IntelliMask Pro/ L-Edit/ Virtuoso/other)

MEMS-CMOS integration design flow can be based on:

- VHDL-AMS
- Verilog-A
- SPICE netlist
- Matlab/Simulink .MEX
What is verification?

Model verification (Schematic vs 3D)
  Verify schematic model and 3D model match
  Ensure MEMS model used in circuit development is accurate

Physical verification (‘Tape Out’)
  Verify physical layout is consistent with Design Rules
  Ensure design meets manufacturability criteria
Static model verification

Pull-in: Schematic results vs Full 3D results
Damping model verification

Perforated condenser membrane

Full capture of fluidic damping and spring force

Full 3D (TEM) vs Macromodel comparison
Dynamic model verification

Transient response of device: Schematic vs FEA (3D)
Tape Out

Physical verification

all angle support

intuitive error markings

Easy error navigation

Tape Out

Physical verification